Time : 3 hours *Full Marks* : 200

Instructions :

*(1) Answer **all** questions following directions.*

(2) The figures in the right-hand margin indicate full marks for the questions.

1. Answer any *two* of the following questions : 10×2=20

(a) Why is NAND gate called a universal gate? Draw the logic diagrams to illustrate how to the following logic gates can be implemented using NAND gate(s) only :

NOT, AND, OR, XOR, XNOR

(b) Draw a state transition diagram for a binary 3-bit up counter. Derive its excitation table and obtain the circuit diagram. Use T flip-flops only.

(c) Obtain the equivalent product-of-sums expansion for the function

$$f(w, x, y, z) = \sum m(1, 3, 4, 5, 10, 12, 13)$$

Simplify $f(w, x, y, z)$ using Karnaugh map.

2. Answer any *two* of the following questions : 10×2=20

(a) Differentiate among class variable, instance variable, automatic variable, static variable and global variable in C++ with suitable examples.

(b) Explain how the binary search algorithm works when searching for element 33 in the following sequence :

0, 12, 28, 42, 55, 87, 91

What is the complexity for a failed search in binary search algorithm?

(c) Explain why a skewed binary search tree is not efficient. How does AVL tree eliminate this inefficiency? Construct an AVL tree by insertion of the following integers :

11, 21, 16, 26, 31, 17, 19, 20

SEAL

3. Answer any *two* of the following questions : 10×2=20

(a) Write down the most natural 8086 addressing modes for the following high-level C statements :

(i) x[i] = y[j];

(ii) int i = *ptr;

(iii) while [*ptr++];

(iv) x = y + 20;

(v) --i;

(b) Using suitable diagrams, explain the architecture of 8085 processor. Explain the significance of the flag register and use of interrupts.

(c) If CS = 1000H, DS = 25A0H, BX = 43A3H, BP = 3400H, find the physical address of the source data for the following instructions :

(i) MOVE AL, [BX + 1200H]

(ii) ADD BL, [BP + 05]

Identify the addressing modes used and its significance.

4. Answer any *two* of the following questions : 10×2=20

(a) Explain the mechanism of dynamic linking with a suitable example. Differentiate between static and dynamic linking.

(b) Explain the various sections of an executable—text, bss and data. Where are the local variables stored in an executable?

(c) Differentiate between absolute loader and relocatable loader, and explain their usage.

5. Answer any *two* of the following questions : 10×2=20

(a) Explain a typical 4-stage instruction pipeline of a RISC processor containing the following stages :

Instruction Fetch, Instruction Decode, Instruction Execute, Writeback

Justify why a 4-stage pipelined processor can experience a speedup of up to 4 times.

(b) The data cache of a computer is implemented as a 4-way set associate cache with a capacity of 256 KB with a block size of 32 bytes. Memory address length is 32 bits.

(i) Compute the size of TAG, SET and OFFSET fields of an address.

(ii) Explain the purpose of VALID bit, MODIFIED bit and REPLACEMENT bit in a cache.

(c) Explain the following terms related to modern computers :

(i) TLB

(ii) Virtual Memory

(iii) Split Cache

(iv) DMA

(v) CISC Machines

6. Answer any *two* of the following questions : 10×2=20

(a) Consider the arrival times and execution times for the following processes in an operating system :

Process	*Execution Time* (ms)	*Arrival Time* (ms)
A	25	0
B	30	20
C	15	35
D	20	50

For the CPU scheduling algorithms Round Robin (time quantum of 5 ms), First Come First Served, Shortest Job First, and Shortest Remaining Time First, compute the following :

(i) The order of completion of processes

(ii) The average waiting time for a process

(b) Explain the limitations of FAT file system. Explain how an inode-base file system solves the limitations of FAT file system.